Notice of Allowability	Application No.	Applicant(s)	
	09/410,928	JONES ET AL.	
	Examiner	Art Unit	
	Brian R. Peugh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the phone interview of 7/26/05*.

2. ☒ The allowed claim(s) is/are *3,4,6,8,11,12,14 and 16*.

3. ☒ The drawings filed on *01 October 1999* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *7/26/05* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Stuart T. Langley, Reg. No. 33,940, on 7/26/05.

The application has been amended as follows:

Cancel claims 1, 2, 5, 7, 9, 10, 13, 15, and 19.

Claim 3, line 1: Replace " The computer system of claim 1" with --A computer system comprising:

a memory system where at least some of the memory is designated as shared memory;

a transaction-based bus coupled to the memory system wherein the transaction-based bus includes a cache coherency transaction defined within its transaction set;

a processor having a cache memory, the processor coupled to the memory system through the transaction based bus;

a plurality of system components other than the processor coupled to the transaction-based bus, wherein the system components access the memory system directly through the transaction based bus, but do not access the cache memory directly through the transaction based bus;

a request issued by one of the plurality of system components and addressed to the processor, wherein the request indicates a request to perform a cache coherency operation; and

wherein the processor is configured to respond to the request by treating the request as an explicit command to perform the cache coherency operation and-- .

Claim 4, line 3: Remove "first".

Claim 4, line 1: Replace " The computer system of claim 1" with --A computer system comprising:

a memory system where at least some of the memory is designated as shared memory;

a transaction-based bus coupled to the memory system wherein the transaction-based bus includes a cache coherency transaction defined within its transaction set;

a processor having a cache memory, the processor coupled to the memory system through the transaction based bus;

a plurality of system components other than the processor coupled to the transaction-based bus, wherein the system components access the memory system directly through the transaction based bus, but do not access the cache memory directly through the transaction based bus;

a request issued by one of the plurality of system components and addressed to the processor, wherein the request indicates a request to perform a cache coherency operation; and

wherein the processor is configured to respond to the request by treating the request as an explicit command to perform the cache coherency operation and-- .

Claim 6, lines 5 and 8: Remove "main".

Claim 6, line 1: Replace "The computer system of claim 5" with --A computer system comprising:

a memory system where at least some of the memory is designated as shared memory;

a transaction-based bus coupled to the memory system wherein the transaction-based bus includes a cache coherency transaction defined within its transaction set;

a processor having a cache memory, the processor coupled to the memory system through the transaction based bus;

a plurality of system components other than the processor coupled to the transaction-based bus, wherein the system components access the memory system directly through the transaction based bus, but do not access the cache memory directly through the transaction based bus;

a request issued by one of the plurality of system components and addressed to the processor, wherein the request indicates a request to perform a cache coherency operation; and

wherein the cache coherency transaction comprises a cache flush transaction and the request includes an address in the shared memory to be flushed from the cache

wherein the processor is configured to respond to the request by treating the request as an explicit command to perform the cache coherency operation and--.

Claim 8, line 1: Replace "The computer system of claim 7" with --A computer system comprising:

a memory system where at least some of the memory is designated as shared memory;

a transaction-based bus coupled to the memory system wherein the transaction-based bus includes a cache coherency transaction defined within its transaction set;

a processor having a cache memory, the processor coupled to the memory system through the transaction based bus;

a plurality of system components other than the processor coupled to the transaction-based bus, wherein the system components access the memory system

directly through the transaction based bus, but do not access the cache memory directly through the transaction based bus;

a request issued by one of the plurality of system components and addressed to the processor, wherein the request indicates a request to perform a cache coherency operation and wherein the processor is configured to respond to the request by treating the request as an explicit command to perform the cache coherency operation;

wherein the cache coherency transaction comprises a cache purge transaction and the request includes an address in the shared memory to be purged from the cache;--.

Claim 11, line 1: Replace "The method of claim 9" with --A method for managing cache coherency in a shared memory system wherein the shared memory system is shared by a plurality of modules, including a processing unit, and wherein the plurality of modules, including the processing unit, are coupled to a system bus, the method comprising the steps of:

causing the processing unit to cache at least some locations of the shared memory system in a cache memory;

initiating a cache coherency transaction on the system bus using one of the plurality of modules other than the processing unit; and

in response to the cache coherency transaction, causing the processing unit to execute a cache coherency operation; and--.

Claim 12, line 1: Replace "The method of claim 9 further comprising:" with --A method for managing cache coherency in a shared memory system wherein the shared memory system is shared by a plurality of modules, including a processing unit, and wherein the plurality of modules, including the processing unit, are coupled to a system bus, the method comprising the steps of:

causing the processing unit to cache at least some locations of the shared memory system in a cache memory;

initiating a cache coherency transaction on the system bus using one of the plurality of modules other than the processing unit; and

in response to the cache coherency transaction, causing the processing unit to execute a cache coherency operation; and--.

Claim 14, line 1: Replace "The method of claim 13" with --A method for managing cache coherency in a shared memory system wherein the shared memory system is shared by a plurality of modules, including a processing unit, and wherein the plurality of modules, including the processing unit, are coupled to a system bus, the method comprising the steps of:

causing the processing unit to cache at least some locations of the shared memory system in a cache memory;

initiating a cache coherency transaction on the system bus using one of the plurality of modules other than the processing unit; and

in response to the cache coherency transaction, causing the processing unit to execute a cache coherency operation; wherein the cache coherency transaction comprises a cache flush transaction and the step of initiating includes indicating an address in the shared memory to be flushed from the cache memory; and--.

Claim 16, line 1: Replace "The method of claim 15" with --A method for managing cache coherency in a shared memory system wherein the shared memory system is shared by a plurality of modules, including a processing unit, and wherein the plurality of modules, including the processing unit, are coupled to a system bus, the method comprising the steps of:

causing the processing unit to cache at least some locations of the shared memory system in a cache memory;

initiating a cache coherency transaction on the system bus using one of the plurality of modules other than the processing unit; and

in response to the cache coherency transaction, causing the processing unit to execute a cache coherency operation; and

wherein the cache coherency transaction comprises a cache purge transaction and the step of initiating includes indicating an address in the shared memory to be purged from the cache memory; and--.

The following is an examiner's statement of reasons for allowance: The prior art including the IDS of June 30, 2002, teach cache coherence systems but fail to teach the combination including the limitation of:

(Claim 3) "...wherein the processor response to the request comprises executing the cache coherency operation without assistance of instructions executed on the processor";

(Claim 4) "...wherein the processor is further configured to respond to the request by generating a response message addressed to the system component that initiated the request indicating status of the cache coherency operation";

(Claim 6) "...when the lookup yields a miss, or a hit to a cache line that is unmodified with regard to the memory system, the processor issues a response to the request immediately; when the lookup yields a hit to a cache line that is modified with

regard to memory, the processor causes a writeback of the specified line to memory followed by a response to the request addressed to the system component that generated the request";

(Claim 8) "...when the lookup yields a hit to a cache line that is modified with regard to the memory system, the processor causes a writeback of the specified line to the memory system followed by an invalidation of the cache line and a response to the request addressed to the system component that generated the request; and when the lookup yields a hit to a cache line that is not modified with regard to the memory system, the processor causes an invalidation of the cache line and a response to the request addressed to the system component that generated the request.

(Claim 11) "...wherein the step of causing the processing unit to execute the cache coherency operation is performed without executing instructions on the processing unit";

(Claim 12) "...generating a response to the initiated cache coherency transaction using the processing unit, wherein the response is addressed to the module that initiated the cache coherency transaction and the response indicates a state of the cache memory";

(Claim 14) "...when the lookup yields a miss, or a hit to a cache line that is unmodified with regard to the shared memory system, issuing a response to the cache coherency transaction immediately; when the lookup yields a hit to a cache line that is modified with regard to the shared memory system, causing a writeback of the specified line to the shared memory system followed by generating a response to the initiated

transaction, wherein the response is addressed to the module that initiated the cache coherency transaction";

(Claim 16) "...when the lookup yields a hit to a cache line that is modified with regard to the shared memory system, causing a writeback of the specified line to the shared memory system followed by an invalidation of the cache line and issuing a response addressed to the module that initiated the cache coherency transaction; and when the lookup yields a hit to a cache line that is not modified with regard to the shared memory system, invalidating the cache line followed by issuing a response addressed to the module that initiated the cache coherency transaction".

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian R. Peugh whose telephone number is (571) 272-4199. The examiner can normally be reached on Monday-Thursday from 7:00am to 4:30pm. The examiner can also be reached on alternate Friday's from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian R. Peugh
Patent Examiner
Art Unit 2187
August 2, 2005